# PCI to Dual UARTs or Printer Port Chip CH351

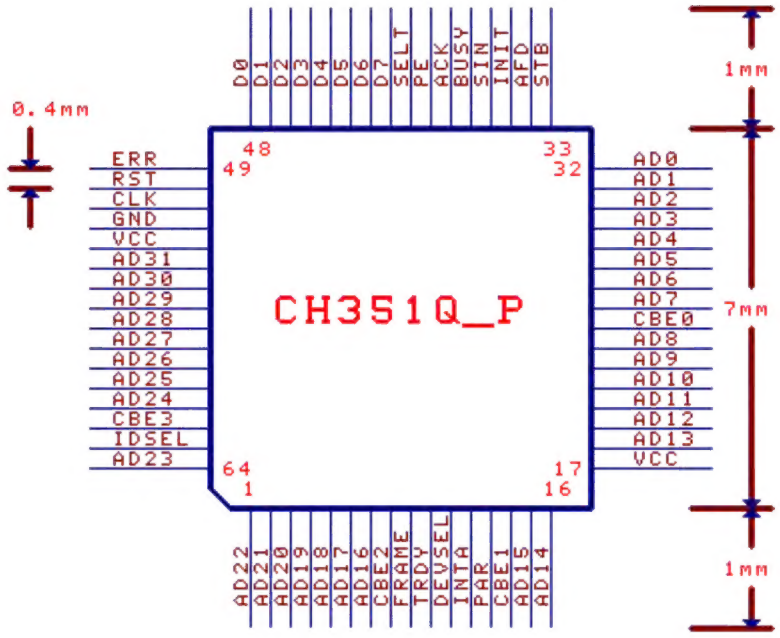
Datasheet (II): Parallel/ Printer port

Version: 1A

http://wch.cn

## 1. Package

Parallel/ Printer port


0.4mm
1mm
7mm
1mm
CH351Q_P
D0 D1 D2 D3 D4 D5 D6 D7 SELT PE ACK BUSY SIN INIT AFD STB
ERR RST CLK GND VCC AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 CBE3 IDSEL AD23
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 CBE0 AD8 AD9 AD10 AD11 AD12 AD13 VCC
AD22 AD21 AD20 AD19 AD18 AD17 AD16 CBE2 FRAME TRDY DEVSEL INTA PAR CBE1 AD15 AD14
48
49
33
32
64
1
17
16

Refer to Datasheet (I) CH351DS1.PDF for the application instructions and pins diagrams of dual UARTs.

## 2. Pin Out

### 2.1. Power line

| Pin No. | Pin Name | Type | Pin Description |
|---|---|---|---|
| 17,53 | VCC | Power | Power supply voltage input |
| 52 | GND | Power | Ground |

### 2.2. PCI Bus Signal Line

| Pin No. | Pin Name | Type | Pin Description |
|---|---|---|---|
| 50 | RST | Input | System reset signal line, active low |
| 51 | CLK | Input | System clock signal line, active at the rising edge |
| 54-61, 64,1-7, 15-16, 18-23, 25-32 | AD31~AD0 | Tri-status output and input | Address and bi-directional data multiplexed signal line |
| 62,8, 14,24 | CBE3~CBE0 | Input | Bus command and byte enable multiplexed signal line |
| 13 | PAR | Tri-status and bi-direction | Odd-even parity signal line |

| | | | |
|---|---|---|---|
| 63 | IDSEL | Input | Initialize device select signal line, active high |
| 9 | FRAME | Input | Frame cycle start signal line, active low |
| 10 | TRDY | Tri-status output | Target device ready signal line, active low |
| 11 | DEVSEL | Tri-status output | Target device select signal line, active low |
| 12 | INTA | Open-drain output | INTA interrupt request signal line, active low |

### 2.3. Printer Port Signal Line

| Pin No. | Pin Name | Type | Pin Description |
|---|---|---|---|
| 41-48 | D7~D0 | Tri-status and bi-direction | 8-bit parallel data output and input, built-in pull-up , connect to DATA7~DATA0 |
| 33 | STB | Output | Data strobe output, active low, connect to STROBE |
| 34 | AFD | Output | Automatic line feed output, active low, connect to AUTO-FEED |
| 35 | INIT | Output | Initialize printer, active low, connect to INIT |
| 36 | SIN | Output | Select printer, active low, connect to SELECT-IN |
| 49 | ERR | Input | Printer error, active low, built-in pull-up, connect to ERROR or FAULT |
| 40 | SELT | Input | Printer online, active high, built-in pull-up, connect to SELECT or SELT |
| 39 | PE | Input | Printer paper empty, active high, built-in pull-up, connect to PEMPTY or PERROR |
| 38 | ACK | Input | Printer data receives response, active at the rising edge, built-in pull-up, connect to ACK |
| 37 | BUSY | Input | Printer busy, active high, built-in pull-up, connect to BUSY |

## 3. Register

For the basic conventions of register, the description of PCI configuration space and bit description of configuration register, please refer to Datasheet (I).

Parallel port of CH351 is compatible with SPP standard printer port with enhanced. The register bits marked in gray in the table are enhanced functions. The actual address of parallel port register is I/O base address 1 adds the offset address in the table. Parallel port of CH351 mainly has four operating modes: SPP (including Nibble, Byte and PS/2), EPP and ECP. ALL in the table indicates all modes, ADV indicates EPP and ECP, RO indicates that register is read-only, WO indicates that register is write-only and R/W indicates that the register is readable and writable.

| Address | Mode | R/W | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | SPP | RO | PIR | D7IN | D6IN | D5IN | D4IN | D3IN | D2IN | D1IN | D0IN |
| 0 | ADV | RO | PIR | IBD7 | IBD6 | IBD5 | IBD4 | IBD3 | IBD2 | IBD1 | IBD0 |
| 0 | ALL | WO | PDR | D7OUT | D6OUT | D5OUT | D4OUT | D3OUT | D2OUT | D1OUT | D0OUT |
| 1 | SPP | RO | PSR | | | | | | !INTFLAG | 1 | 1 |
| 1 | EPP | RO | PSR | !BUSY | ACK | PE | SELT | ERR | 1 | 1 | !EPPREQ |
| 1 | ECP | RO | PSR | | | | | | !ECPICMD | !ECPIBF | !ECPOUT |
| 2 | ALL | R/W | PCR | 1 | 1 | DIRIN | INTEN | !SIN | INIT | !AFD | !STB |
| 3 | SPP | R/W | PXR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | EPP | R/W | PXR | 0 | 0 | 0 | 0 | EPPADDR | MODEEPP | 0 | 0 |
| 3 | ECP | R/W | PXR | 0 | 0 | 0 | ECPINTF | 0 | 0 | ECPDIRIN | MODEECP |

The following table shows default of parallel port register after power-on reset or PCI bus reset.

| Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| PIR | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| PDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PSR | !BUSY | ACK | PE | SELT | ERR | 1 | 1 | 1 |
| PCR | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| PXR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PIR: data input register, used to input real-time data from D7-D0 pins in SPP mode. In EPP or ECP mode, the data which has been latched input /uploaded to buffer. In EPP mode, the data is latched when AFD pin or SIN pin outputs a low level; in ECP mode, the data is latched when ACK pin is at the low level, and !ECPICMD is also latched at the same time.

PDR: data output register, used to write data to be outputted /downloaded. Writing into this register in SPP mode, and the data will be directly outputted to D7-D0 pins; writing into this register in EPP or ECP mode, and the handshake protocol of data output or data input will be automatically executed.

PSR: status register, used to query the input pin and operate the execution status.

!BUSY: this bit is the reverse value of the status of the input pin BUSY in SPP, EPP and ECP modes. When BUSY pin inputs a high level, this bit is 0.

ACK: this bit is the status of the input pin ACK in SPP, EPP and ECP modes.

PE: this bit is the status of the input pin PE in SPP, EPP and ECP modes.

SELT: this bit is the status of the input pin SELT in SPP, EPP and ECP modes.

ERR: this bit is the status of the input pin ERR in SPP, EPP and ECP modes.

!INTFLAG: this bit is the reverse value of the interrupt flag in SPP mode. When the rising edge of the ACK pin generates an interrupt flag, this bit will be automatically cleared to 0, and will be automatically set to 1 after reading PSR register.

!EPPREQ: this bit is the reverse value of the access operation proceeding flag in EPP mode. When writing into PDR register, this bit will be automatically cleared to 0 and attempting EPP access operation. This bit will be automatically set to 1 until the operation is completed.

!ECPICMD: this bit is the reverse value of the command flag during reverse transmission in ECP mode. When the reverse transmission is a command, this bit is 0.

!ECPIBF: this bit is the reverse value of the upload buffer full flag for reverse transmission in ECP mode. When the upload buffer is full, this bit will be automatically cleared to 0, and it will be automatically set to 1 after reading PIR register.

!ECPOUT: this bit is the reverse value of the forward transmission operation proceeding in EPP mode. When writing into PDR register, this bit will be automatically cleared to 0 and attempting EPP forward output operation. This bit will be automatically set to 1 until the operation is completed.

PCR: control register, used to control the output pin, transmission direction and interrupt enabling.

DIRIN: this bit is the tri-status output control of the bi-directional data lines D7-D0 in SPP, EPP and ECP modes. When it is cleared to 0, it means that the D7-D0 pins allow tri-status output. When it is set to 1, it means that D7-D0 pins disable tri-status output.

INTEN: this bit is the PCI interrupt output enabling. When it is set to 1, the output of interrupt request is allowed; when it is cleared to 0, the output of interrupt request will be disabled.

!SIN: bit=1, SIN pin output is valid (active low), otherwise, SIN pin output is invalid.

INIT: bit=1, INIT pin output is invalid, otherwise, INIT pin output is valid (active low).

!AFD: bit=1, AFD pin output is valid (active low), otherwise, AFD pin output is invalid.

!STB: bit=1, STB pin output is valid (active low), otherwise, STB pin output is invalid.

PXR: configuration register, used to set the operating mode of parallel port.

EPPADDR: this bit is the target space selection in EPP mode. When it is 1, it corresponds to the address access operation of EPP. When it is 0, it corresponds to the data access operation of EPP.

MODEEPP: bit=1, enabling EPP mode.

ECPINTF: this bit is an interrupt flag in ECP mode. When the falling edge of ERR pin generates an interrupt flag, this bit will be automatically set to 1, and it will be automatically cleared to 0 after reading PXR register.

ECPDIRIN: this bit is the transmission direction control in ECP mode. When it is 0, it corresponds to ECP forward transmission/output. When it is 1, it corresponds to ECP reverse transmission/input.

MODEECP: bit=1, enabling EPP mode.

# 4. Functional Specifications

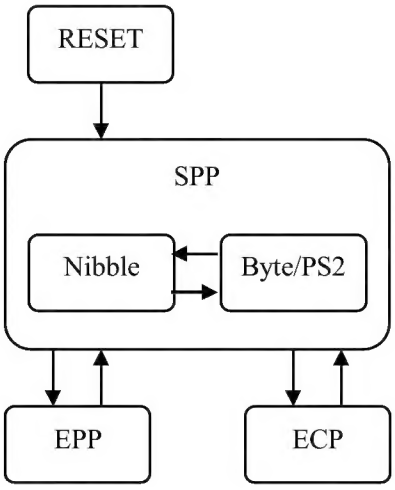
## 4.1. Query and Interrupt

Parallel port of CH351 uses a PCI interrupt request pin, so after entering PCI interrupt service, firstly analyzing whether it is CH351 request interrupt and then process it. After entering the interrupt service, reading PSR or PXR register of parallel port firstly. If it is in ECP mode, checking ECPINTF flag of PXR register, otherwise, checking !INTFLAG flag of PSR register. If it is valid, it means there is an interrupt and exit it after processing, it is invalid, it means there is no interrupt and exit it directly.

If parallel port works in interrupt mode, then setting the INTEN of PCR register to allow interrupt output. SPP or EPP mode enables the interrupt request by the rising edge of ACK pin, and ECP mode enables the interrupt request by the falling edge of ERR pin. If parallel port works in the query mode, then do not to set the INTEN of PCR, and only need to query PSR and PXR registers, and analyze and process it.

## 4.2. Parallel Port Operation

The three operating modes of CH351 parallel port are mutually exclusive, and it is SPP mode by default. In SPP mode, it can realize an additional mode such as Nibble, Byte, PS/2, etc. PXR register can also be set to switch back and forth between SPP, EPP or ECP modes. In SPP mode, software can be used to control PCR and query PSR to realize transmission of Nibble, Byte and PS/2, etc. Refer to IEEE1284 specifications for the specific operation. The operating mode switching diagram of parallel port is as shown below.




## 4.3. Application Specification

Parallel port's output pins of CH351 are all CMOS level, compatible with TTL level, the input pins are compatible with CMOS land TTL level, and the input pins have built-in pull-up resistors required by the printer port, which can simplify the peripheral circuit.

The pins of CH351 in parallel mode include: bi-directional data pins, control output pins and status input pins. Except INIT pin, the bi-directional data pin and control output pin are all at high level by default. In SPP mode, all signals can be used as general-purpose IO pins, controlled and defined usage by the computer application.

In Windows and Linux OS, the drive of CH351 can be compatible with standard printer ports, so most of the original parallel port applications are completely compatible and without any modification.

CH351 can be used to expand additional high-speed RS232 serial port and parallel printer ports for computer through PCI bus.

# 5. Parameters

## 5.1. Absolute Maximum Ratings

(Critical state or exceeding maximum can cause chip to not work or even be damaged)

| Name | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| TA | Operating ambient temperature | -40 | 85 | ℃ |
| TS | Storage ambient temperature | -55 | 125 | ℃ |
| VCC | Supply voltage (VCC connects to power, GND to ground) | -0.5 | 6.0 | V |
| VIO | Voltage of the input or output pins | -0.5 | VCC+0.5 | V |

## 5.2. Electrical Parameters

(Test Conditions: TA=25℃, VCC=5V, exclude pins connected to PCI bus)

| Name | Parameter Description | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| VCC | Supply voltage<br>(please refer to the attention below) | 4.5 | 5 | 5.3 | V |
| ICC | Operating supply current | 1 | 15 | 50 | mA |
| VIL | Input low voltage | -0.5 | | 0.8 | V |
| VIH | Input high voltage | 2.0 | | VCC+0.5 | V |
| VOL | Output low voltage (4mA draw current) | | | 0.5 | V |
| VOH | Output high voltage (1mA output current) | VCC-0.5 | | | V |
| IIN | Input current of the input without pull-up | | | 10 | uA |
| IUP | Input current of the input with pull-up | 100 | 250 | 500 | uA |

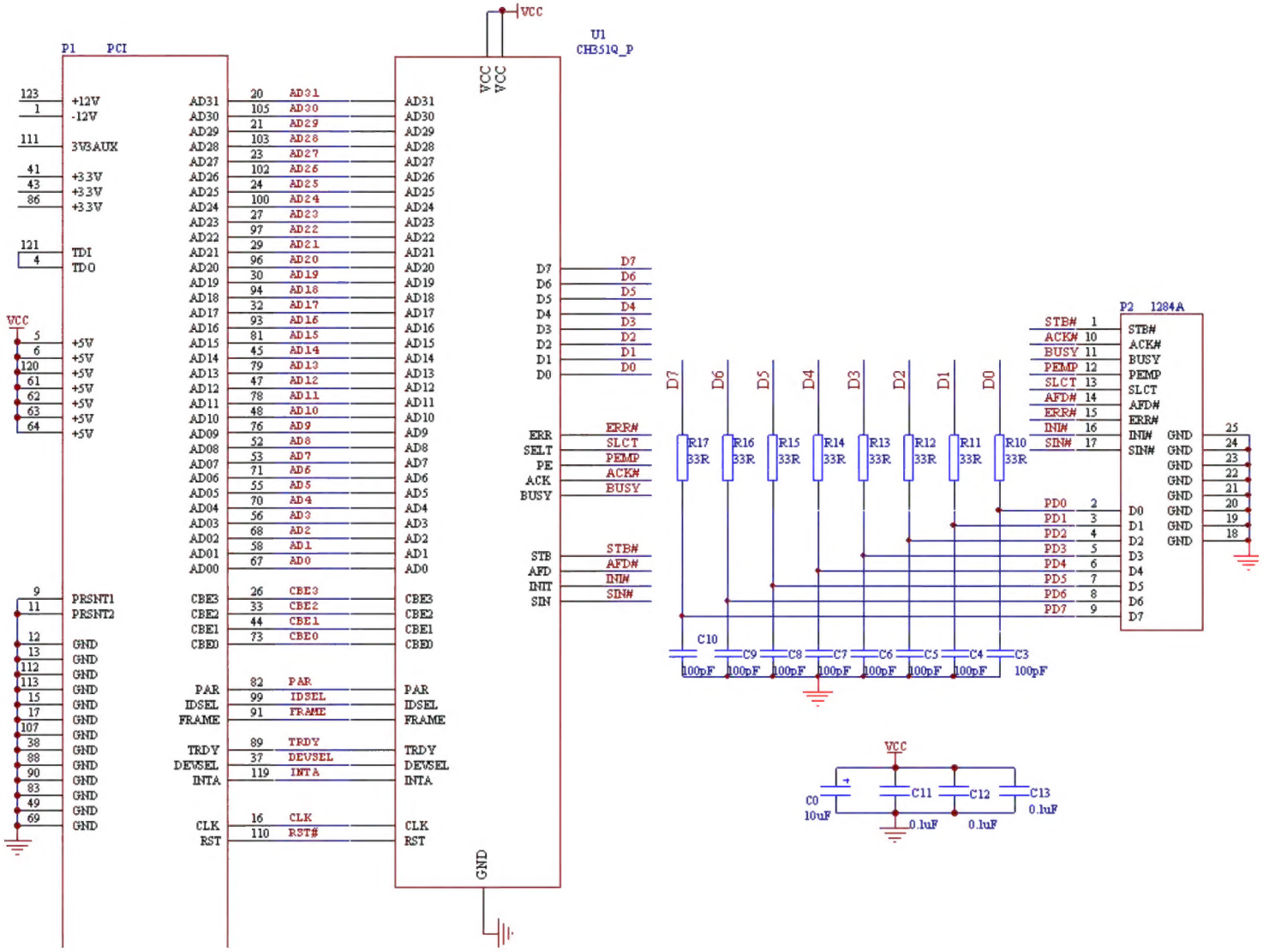
## 5.3. Timing Parameters

(Test Conditions: TA=25℃, VCC=5V, FCLK=33.3MHz)

| Name | Parameter Description | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| FCLK | CLK input frequency (main frequency of PCI bus) | 0 | 33.3 | 40 | MHz |

# 6. Application

## 6.1. Parallel/Printer Port

This is a parallel/printer port circuit based on the CH351. P2 is the type A DB25 hole of IEEE1284 (print port connector). The series resistors R10~R17 and the parallel capacitors C3~C10 are used for impedance matching of parallel port data line, and they cannot need if the requirement is not high. Capacitors C0 and C11~C13 are used for power decoupling. C11~C13 are monolithic or high-frequency ceramic capacitors with a capacity of 0.1uF. They are connected in parallel nearby to the power pins of CH351 separately.

CH351 is a high-frequency digital circuit, so signal impedance matching shall be considered. Please refer to PCI bus specification when designing the PCB board. It is recommended that the length of PCI signal line of CH351 shall be less than 35mm and the length of clock line CLK try to be between 50mm~65mm, and it shall not be close to other signal lines. It is recommended to arrange ground or copper on both sides of CLK and on the back of PCB to reduce signal interference from the outside.